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HIGH-FREQUENCY HIGH-VOLTAGE HIGH-POWER DC-TO-DC CONVERTERS

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1. Introduction

Building on the pioneering work of the space program in applying semiconductor switching techniques to process power where size, weight, efficiency, and reliability are of utmost concern, the number of applications of this technology to aerospace, military and industry needs has increased at a dramatic rate in recent years. As with most new technologies, initial successes have been rewarded with pressure to extend the range of operating conditions and applications of switching converters. In the case of dc-to-dc power conditioners, this pressure is toward higher conversion frequencies to reduce the size and weight of the reactive components, higher voltage levels, as in off-of-the-line power systems, and higher power levels.

The research upon which this paper is based is motivated by the need foreseen by the USA National Aeronautics and Space Administration for spacecraft with solar array generation and power conditioning capability in the range of hundreds of kilowatts. Envisioned is a power conditioning system using three-wire dc distribution with the relatively high line-to-common voltages of ±500 volts chosen to reduce size and weight of the conductor system. The source of power is intended to be a solar-cell array reflecting a reasonable balance between series and parallel cell connections with a dc input voltage range of 100 to 200 volts. Research to date has focused on single power-stage dc-to-dc modules operating in the 2.5-kW range at a switching frequency of 100 kHz with an input voltage of 110 V to 180 V and an output voltage of 250 V. These requirements press today's technology simultaneously on all three fronts -- high frequency, high voltage and high power. Accomodating to the limiting constraints on one front typically leads to problems on another.

Trade-off determinations involving converter size, weight, efficiency and reliability with respect to conversion frequency, input and output voltages, and increased load power is an extremely complex issue. In the material to follow, attention is directed particularly to the implications that the simultaneous requirements of high-frequency (H-F), high-voltage (H-V), and high-power (H-P) operation have on the power switching transistors, on the power diodes, and on circuits designed to protect them.

2. Implications of H-F H-V H-P Operation on Power Switching Transistors

During the past few years, power switching transistors, both bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs), have been developed that can switch high voltages and high currents in very short periods of time. These recent developments have created the potential for operating high-voltage high-power dc-to-dc converters at switching frequencies in the range of 100 kHz and beyond. However, as transistor switch-

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Table 1. Example Converter Parameters			Table 2. Power Transistor Parameters	
V_I = 140 V	V_O = 250 V	N_P/N_S = 1/2	MOSFET t_{fv} = 50 ns	BJT t_{fv} = 50 ns
I_{PA} = 28 A	I_{PB} = 40 A	f_S = 100 kHz	t_{fi} = 50 ns	t_{fi} = 100 ns
$I_{P,AV}$ = 17 A		$I_{P,RMS}$ = 24.2 A	$R_{D(ON)}$ = 0.1 Ω	$V_{CE(SAT)}$=0.6V

ing times become shorter, time rates of change of current di/dt becomes higher, and even small parasitic inductances such as stray lead inductance and/or transformer leakage inductance can cause serious transistor overvoltage problems at turn-off. It therefore becomes necessary to understand the full effects of parasitic inductance on the power switching transistor in order to effectively design transistor protection circuitry to maintain high reliability and maximize overall converter efficiency.

The discussion and analysis in this section and in the following sections focus on a two-winding current-or-voltage step-up (buck-boost) converter shown in Fig. 1, although the principles presented are applicable to all three basic types of energy-storage dc-to-dc converters. Where appropriate, numerical examples are based on the converter parameters presented in Table 1. The parameter values given in Table 1, as well as other example parameter values presented in this paper, correspond to data drawn from the operation of experimental current-or-voltage step-up power stages operating at output power levels of up to 2 kW and higher. Also, where appropriate, discussion is directed at both BJTs and MOSFETs, and the example parameters associated with the two types of devices are given in Table 2. As before, this data reflects experimental observations. It should be noted that these transistor parameters are not based on a single commercially available device, but represent the parallel combination of four transistors in the MOSFET case and two transistors in the BJT case.

To provide a basis for examining the full effects of parasitic inductance on the power transistor, we begin by examining the transistor voltage and current waveforms for the purely hypothetical case where there is no parasitic series inductance, i.e., $L_{P,PAR}$ and $L_{S,PAR}$ in Fig. 1 are zero. The solid line in Fig. 2 depicts the associated idealized switching trajectory in the i_Q vs. v_Q plane for the power transistor Q in Fig. 1 for the case of continuous mmf where the reactor mmf is considered to be nonzero at all times. The dashed line represents the typical reverse-bias safe operating area (RBSOA) for a BJT and serves to emphasize the fact that the inductive switching trajectory of the transistor may well lie outside the RBSOA of a BJT.

Figure 3 depicts the corresponding idealized time-domain waveshapes of i_Q and v_Q. During the time the transistor Q is ON and the secondary-circuit diode D is OFF, the primary-circuit current increases linearly from $I_{PA} = \mathcal{F}_A/N_P$ to $I_{PB} = \mathcal{F}_B/N_P$. During the very short time intervals when Q and D are turning ON and OFF, it is assumed the net mmf of the reactor $\mathcal{F} = N_P i_Q + N_S i_D$ remains essentially constant. Therefore, when parasitic inductance is not present, i_Q at turn-on must rise to its initial value I_{PA} before D becomes nonconducting and v_Q can begin to fall; at turn-off, v_Q must rise to the value $V_{Q,OFF} = V_I + (N_P/N_S)V_O$ before D is turned ON and I_Q can begin to fall from its peak value of I_{PB}. This latter condition at turn-off exists regardless of the presence of parasitic inductance. To simplify the analysis, the fall of v_Q at

turn-on and the fall of i_Q at turn-off are assumed to be linear functions of time, and these intervals are designated t_{fv} and t_{fi}, respectively.

We now turn our attention to the case where the effects of parasitic series inductance are included in the analysis of the transistor waveshapes. This parasitic series inductance, whether due to transformer leakage inductance or to stray inductance resulting from excessive circuit lead lengths anywhere in the primary or secondary side of the converter circuit, is normally distributed in nature. For the purpose of analysis, the distributed parasitic series inductance L_{PAR} can be treated as a single lumped element, and referred to either the primary or secondary side of the circuit. For discussion purposes, when this parasitic series inductance L_{PAR} is referred to the primary side of the converter circuit, it is designated $L_{P,PAR}$. When the parasitic inductance is referred to the secondary side of the circuit, it is designated $L_{S,PAR}$. The value of the distributed parasitic inductance may range from a few nanohenries for a circuit with short lead lengths and without transformer coupling, to several microhenries when transformer coupling is used, as in the two-winding current-or-voltage step-up converter discussed here. The effects of parasitic inductance appear during the turn-on switching interval as well as during the turn-off switching interval of the transistor Q. These effects result in the altered switching trajectory depicted by the dotted line in Fig. 2, with the corresponding current and voltage waveshapes in the time domain shown in Fig. 4, where linear transistor switching is again assumed..

It was mentioned that during the turn-on interval for the case where there are no parasitic inductive effects, the transistor current must rise to the value I_{PA} before the secondary diode D becomes nonconducting and the transistor voltage can begin to fall. With circuit parasitic inductances no longer considered zero, i_Q can no longer rise instantaneously to the value I_{PA} at the beginning of the turn-on interval. Neglecting the forward drop of diode D, the voltage across $L_{P,PAR}$ during the interval t_{fv} is $v_{LP,PAR} = V_{Q,OFF} - v_Q = V_I + (N_P/N_S)V_O - v_Q$.

We see that, during the initial portion of the turn-on interval, the transistor voltage is no longer held at $V_{Q,OFF}$ until i_Q rises to the value I_{PA}, but drops at a linear rate which is mirrored by a linear voltage rise across $L_{P,PAR}$. The resulting current i_Q thus rises parabolically during the interval t_{fv}. When v_Q has dropped to its low ON-time value at the end of the interval t_{fv}, i_Q continues its rise, but at a linear rate according to the approximate relationship $di_Q/dt = V_{Q,OFF}/L_{P,PAR}$ until the point where i_Q reaches I_{PA}.

When parasitic inductance is small and turn-on switching loss is excessive, a lumped series inductance is often purposely added in the form of a series turn-on snubber to reduce the power loss during this interval. A discussion and analysis of series turn-on snubbers can be found in Ref. [1]. For the time being, it is assumed that $L_{P,PAR}$ is large enough, as in the case where transformer coupling is utilized, that further shaping of the transistor turn-on trajectory is unnecessary.

Comparing the waveshapes of i_Q and v_Q during turn-on in Figs. 3 and 4, the presence of parasitic inductance is seen to lower the switching loss during this interval, but serves also to increase switching loss during the turn-off interval. Just prior to the instant of time when the transistor current begins to fall, the energy stored in $L_{P,PAR}$ is $W_{LP,PAR} = L_{P,PAR} I_{PB}^2/2$. If no other means for dissipating this energy are available, it must be dissipated in the transistor during the current fall time t_{fi}. In our example converter, assume that through the use of special transformer winding techniques and careful

attention to circuit lead lengths, the value of $L_{P,PAR}$ is 500 nH. At a switching frequency of 100 kHz, the extra power which must be dissipated by the power transistor at turn-off is $L_{P,PAR} I_{PB} f_S/2$ or about 40 W. While the magnitude of this increase in transistor turn-off power dissipation, which obviously degrades converter efficiency, may not in itself prohibit the successful operation of the power switching transistor, there is a second and far more deleterious effect caused by the presence of $L_{P,PAR}$.

In Fig. 4, we see that during the current fall time of Q, there is a voltage overshoot equal to $L_{P,PAR}(di_Q/dt)$. Following our assumption of a linear current fall time, the peak voltage which the transistor must withstand during the turn-off interval is $V_{Q,peak} = V_{Q,OFF} + L_{P,PAR} I_{PB}/t_{fi}$. In the BJT example, this amounts to a peak transistor voltage of approximately 465 V, whereas in the MOSFET case, the peak voltage is approximately 665 V.

In practice, the rate at which the transistor current falls to zero is usually greater during some portion of the interval t_{fi} than the rate suggested by assuming linear switching, and the magnitude of the voltage overshoot observed in an actual circuit is greater than the magnitude predicted in the preceding analysis. In any case, the breakdown voltage ratings of commercially available transistors possessing switching times fast enough for operation at 100 kHz and higher generally fall in the range of 400 V to 500 V. We are then presented with an interesting dilemma. The fast speed of recently-developed power switching transistors, which enables high-frequency operation without excessive transistor power dissipation, at the same time contributes to excessive voltage stress due to the presence of parasitic series inductance. In Section 4, we examine possible solutions to this problem.

3. Implications of H-F H-V H-P Operation on Power Diodes

All three basic types of energy-storage dc-to-dc converters -- current step-up, voltage step-up, and current-or-voltage step-up -- rely on a power diode to provide a path for energy transfer from the energy-storage reactor to the load during the OFF-time of the power switching transistor. Furthermore, the manner in which the diode behaves during its reverse-recovery period profoundly affects not only the stresses placed on the diode but on the transistor as well.

For convenience in examining diode stresses, the effective composite parasitic series inductance is now referred to the secondary side of the converter and is designated by the lumped inductance $L_{S,PAR}$. To understand the behavior of the diode D and its relationship to other converter phenomena, it is necessary to understand the diode current and voltage waveforms depicted in Fig. 5, where the corresponding transistor current and voltage waveforms have also been included to illustrate the correlation between the two sets of waveforms, as well as to illustrate the effects of diode reverse-recovery time on the transistor waveshapes.

At the time designated t_0 in Fig. 5, the diode D becomes forward-biased, and the diode current i_D rises to the value $I_{SB} = \mathcal{F}_B/N_S$ at time t_1. The rise of i_D mirrors the fall of the transistor current i_Q from I_{PB} to zero, and therefore $t_1 - t_0 = t_{fi}$, the transistor current fall-time. From t_1 to t_2 the diode current ramps down linearly to the value $I_{SA} = \mathcal{F}_A/N_S$ as the energy-storage reactor releases energy to the load. At t_2, the transistor Q starts to turn ON, and the rise of transistor current i_Q is mirrored by a fall in i_D until t_3 when the transistor voltage v_Q has fallen to its low ON-time value. Therefore,

$t_3 - t_2 = t_{fv}$, the transistor voltage fall time.

Beginning at t_3, i_D decreases linearly at a rate $di_D/dt = V_{D,OFF}/L_{S,PAR}$ where $V_{D,OFF} = (N_S/N_P)\,V_I + V_O$, until at t_5 a peak reverse diode current $I_{DR,peak}$ is reached, and the diode begins to support reverse voltage. During the time interval from t_5 until t_6, designated as t_{R2} in Fig. 5, the diode current falls back to zero, while the diode voltage reaches a peak reverse value $V_{DR,peak}$ before settling back to the diode OFF-voltage $V_{D,OFF}$. The exact shape of the current and voltage waveforms during the time interval t_{R2} are dependent on the dynamics of the diode as well as the circuit external to the diode. However, for the purpose of obtaining a very rough estimate of the peak diode reverse voltage $V_{DR,peak}$, let us assume that the diode current falls linearly with respect to time during the interval t_{R2}, and the diode reverse voltage rises instantaneously. Again drawing on experimental observation, assume $L_{S,PAR} = 2.0\,\mu H$, $I_{DR,peak} = 15$ A and $t_{R2} = 50$ ns. The peak diode reverse voltage can then be estimated as $V_{DR,peak} = V_{D,OFF} + L_{S,PAR}\,I_{DR,peak}/t_{R2} = 530$ V + 600 V = 1130 V.

As with the peak transistor voltage calculated for the interval t_{fi}, the above estimate for $V_{DR,peak}$ is likely to be lower than the experimentally observed value, since the diode current generally falls at some point in the interval t_{R2} at a rate faster than the rate predicted by a linear fall time. Note also that the energy $L_{S,PAR}\,I^2_{DR,peak}/2$ stored in the parasitic series inductance at time t_5 must be dissipated principally by the diode during the the interval t_{R2}, adding to the total power dissipation of the diode and degrading overall converter efficiency. Another detrimental effect due to diode reverse-recovery time is that the peak transistor current at turn-on becomes $I_{PA} + (N_S/N_P)I_{DR,peak}$, and unless sufficient transistor drive is available during this interval, the transistor forward voltage will rise with a corresponding increase in transistor power dissipation.

Because the peak diode reverse current $I_{DR,peak}$ profoundly influences not only the power dissipation and voltage stresses placed on the diode itself, but determines the magnitude of the current stress placed on the power switching transistor during its turn-on interval, it is of interest to examine the relationship between the parasitic series inductance $L_{S,PAR}$ and the parameter $I_{DR,peak}$.

Referring again to Fig. 5, assume that at time t_4 when the diode current is crossing the zero-axis, the stored charge in the diode is of magnitude q_0. Since q_0 must equal the integral of $i_D(t)$ from t_4 to t_5, we have $q_0 = \int_{t_4}^{t_5} i_D(t)\,dt = I_{DR,peak}\,t_{R1}/2$. In addition, we have $di_D/dt = I_{DR,peak}/t_{R1} = V_{D,OFF}/L_{S,PAR}$ which can be solved for t_{R1} and substituted into the expression for q_0 yielding the result $L_{S,PAR}\,I^2_{DR,peak}/2 = q_0 V_{D,OFF}$. This equation might seem to imply that the energy stored in the parasitic series inductance at time t_5 is independent of $L_{S,PAR}$, and only depends on the magnitude of the stored charge and the OFF-voltage of the diode. Such a conclusion, however, is not true in general, since the magnitude of the stored charge is dependent not only on the level of forward diode current immediately preceding the onset of commutation, but on the time rate of change of current di_D/dt immediately following the onset of commutation. As a consequence, the magnitude of the stored charge depends strongly on the magnitude of the parasitic series inductance for many cases. However, the published curves of Von Zastrow and Galloway [2] suggest that for very large time rates of change of current ($di_D/dt > 20$ A/μs), a case

applicable to high-frequency high-voltage high-power converters, the stored charge is essentially independent of dip/dt. The magnitude of dip/dt in our example converter is 265 A/μs. In this case, it is therefore unlikely that purposely increasing the series parasitic inductance will lead to a proportionate decrease in stored charge. We can be certain, however, that the above charge will lead to a proportionate increase in the amount of energy stored in the parasitic series inductance immediately prior to the beginning of the power switching transistor turn-off interval. In general, there exists a very real trade-off between the transistor turn-on switching loss, the transistor turn-off switching loss, and the diode switching loss as they are affected by the magnitude of the parasitic series inductance, and this trade-off must be carefully considered if efficiency is to be maximized.

With the above effects in mind, the selection of the proper power diode now becomes of critical importance. All other conditions being equal, diodes specified as having shorter reverse-recovery times exhibit smaller peak reverse-recovery currents [3]. Generally speaking, however, specified reverse-recovery time increases with specified breakdown voltage for commercially available diodes. Therefore, we are again presented with a dilemma. In order to keep diode power dissipation at a minimum, and overall converter efficiency at a maximum, we are forced to use diodes with the fastest reverse-recovery times available. At the same time, these diodes possess lower reverse-voltage ratings than their slower counterparts, and consequently are less capable of withstanding the types of voltage transients occuring in a high-voltage high-power converter. The answer to this problem lies in the ability to protect the power diode from inductive voltage transients, a topic which is discussed in the next section.

4. Semiconductor Switch Protection Circuitry Design Considerations

From the discussion concerning the various stresses placed upon the semiconductor switches in a H-F H-V H-P environment, it is evident that a crucial function which must be performed by the semiconductor switch protection circuitry is that of controlling the peak voltage appearing across the switch so as to prevent the voltage rating of the switch from being exceeded when it is turned OFF. In the case where a BJT is utilized as the power switch, an equally important function of the semiconductor switch protection circuit is to shape the switching trajectory to contain it within the boundaries imposed by the RBSOA of the device as it is turned OFF. This section, therefore, focuses on the design of semiconductor switch turn-off protection circuitry as it relates to H-F H-V H-P operation and to efficiency. The vehicle for discussion, as before, is the two-winding current-or-voltage step-up converter, which is assumed to contain significant amounts of distributed parasitic series inductance.

Figures 6(a), (b), and (c) depict several methods out of a variety of possibilities for protecting the semiconductor switches during their respective turn-off intervals. In Fig. 6(a), both the transistor and the diode are protected by RC-type turn-off snubbers. In Fig. 6(b), the switches are protected by RC-type voltage clamps. In Fig. 6(c), the transistor is protected by an LC-type snubber. The authors are unaware of a comparable LC-type protection circuit for the power diode. Detailed discussions of the design and analysis of the protection circuits depicted in Figs. 6(a) to (c) are available in the literature [1][4][5]. The purpose here is to examine some of the salient

features of each type of protection circuit as they relate to H-F H-V H-P operation.

We begin our discussion with the protection circuits associated with the power switching transistor. All three circuits -- the RC-type snubber, the RC-type clamp, and the LC-type snubber -- can be designed to limit the peak transistor voltage $V_{Q,peak}$ to some specified maximum value $V_{Q,MAX}$, which is determined by the voltage rating of the device and safety-margin considerations. In addition, the RC-type and LC-type snubbers can be designed to provide the waveshaping action necessary to contain the switching trajectory within the RBSOA of a BJT. In general, if snubber capacitance is sized to limit the transistor voltage to some value $V_{Q,MAX}$, the snubber will provide more than the amount of waveshaping action necessary to satisfy RBSOA limitations unless $V_{Q,MAX}$ is unusually large and the RBSOA is unusually small. The use of an RC-type clamp, however, does not guarantee that RBSOA limitations are not exceeded, as illustrated in Fig. 7, where the effects of the various protection circuits on the transistor switching trajectory are shown.

The function of all three protection circuits is to redirect the flow of the energy $W_{LP,PAR} = L_{P,PAR} I_{PB}^2/2$ stored in the parasitic series inductance immediately prior to the turn-off of the power transistor away from the transistor. In providing this means, all three circuits must store more energy during the transistor turn-off interval, by means of the protection circuit capacitances, than the amount of energy $W_{LP,PAR}$ stored in the parasitic inductance.

In the case of the RC-type snubber and the RC-type clamp, the energy stored by the snubber or the clamp during the transistor turn-off interval is dissipated primarily in the snubber resistor or the clamp resistor. The overall power dissipation (transistor plus protection circuit) resulting from utilizing RC-type protective circuits in a H-F H-V H-P environment can range into the hundreds of watts, profoundly reducing overall converter efficiency.

In the case of the LC-type snubber, the energy absorbed by the snubber capacitor is partially circulated between the snubber capacitor and the snubber inductor, and partially returned to the input source, which must be capable of absorbing this returned energy. Although the LC-type snubber is sometimes referred to as a "nondissipative" snubber, this label is somewhat misleading. The energy stored in the snubber capacitor during the transistor turn-off interval must be circulated through circuit components which are nonideal both statically and dynamically. In particular, the forward voltage drops of the snubber diodes and the power transistor, the losses in the snubber inductor, and the reverse-recovery losses in the snubber diodes are all principal contributors to an overall power loss in the LC-type snubber, and as the energy which must be circulated through these elements increases, so does this power loss. It is difficult to accurately predict the losses associated with the LC-type snubber, primarily because of the complex dynamic behavior of the snubber components. It would be reasonable to expect, however, that because only a portion of the energy stored in the snubber capacitor is dissipated, the overall power loss incurred through the use of the LC-type snubber will be less than that incurred when either RC-type protection circuit is used. The lower expected power dissipation of the LC-type snubber makes it the more logical choice for protecting the power transistor in a H-F H-V H-P environment.

Turning to the protection of the power diode D, since a low-loss protection circuit such as the LC-type snubber apparently is not available for use in conjunction with the diode, it is expected that the turn-off protection

of the power diode will be at the expense of a considerable amount of power dissipation. Fortunately, with a fast-recovery diode, the energy $W_{LS,PAR} = L_{S,PAR} I_{DR,peak}^2/2$ which must be controlled by the diode protection circuitry is likely to be considerably less than the energy $W_{LP,PAR}$ which must be controlled by the power transistor protection circuitry.

As in the case of RC-type protection circuitry for the transistor, both diode protection circuits are required to store more energy during the reverse-recovery time of the power diode, by means of the protection circuit capacitor, than $W_{LS,PAR}$. Because the energy stored by the protection circuit capacitor is eventually dissipated in the protection circuit resistive element, the proper selection of power diode protection circuitry is of critical importance in maximizing converter efficiency.

Recall that to obtain low peak reverse-recovery currents, it is necessary to choose diodes with short reverse-recovery times and correspondingly low reverse-voltage capability. Commercially-available diodes suitable for high-frequency operation presently have reverse-voltage ratings less than 1000 V. It can be shown that in some cases, particularly where the ratio of the maximum allowable diode reverse voltage $V_{DR,MAX}$ to diode OFF voltage $V_{D,OFF}$ is small, i.e., $V_{D,MAX}/V_{D,OFF} < 2$, the energy which must be stored by the clamp circuit during the reverse-recovery time of the power diode is significantly less than what must be stored by the snubber circuit. However, due to the nonlinear behavior of the power diode during the time interval t_{R2}, it is difficult to predict precisely how the use of either circuit affects the switching loss in the power diode. Consequently, the best judgements concerning diode protection circuitry usually have to be based on experimental observation.

5. Conclusion

A simple analysis of the current and voltage waveshapes associated with the power transistor and the power diode in an example current-or-voltage step-up (buck-boost) converter is presented. The purpose of this analysis is to highlight the problems and possible trade-offs involved in the design of high-voltage high-power converters operating at switching frequencies in the range of 100 kHz. It is seen that although the fast switching speeds of currently available power diodes and transistors permit converter operation at high switching frequencies, the resulting time rates of change of current (di/dt), coupled with parasitic inductances in series with the semiconductor switches, produce large repetitive voltage transients across the semiconductor switches, potentially far in excess of the device voltage ratings. The need is established for semiconductor switch protection circuitry to control the peak voltages appearing across the semiconductor switches, as well as to provide whatever waveshaping action is required for a given type of semiconductor device.

The process of maximizing the efficiency of such a high-frequency high-voltage high-power converter involves a complex set of trade-offs, not all of which are well understood or easily quantifiable due to the nonlinear behavior of the circuit components involved. The purpose here is to enumerate the possible trade-offs, as well as the various factors influencing these trade-offs, that must be considered in order to maximize the efficiency of high-frequency high-voltage high-power converters.

6. References

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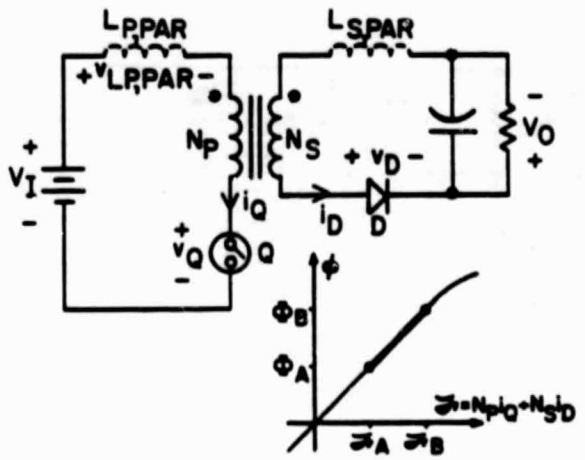


Fig. 1

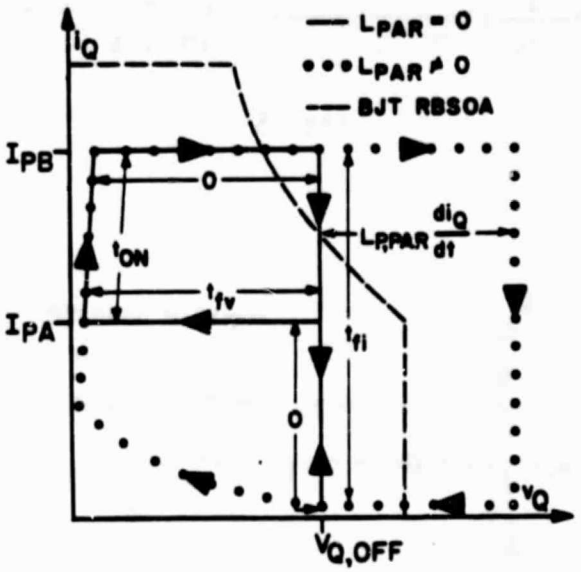


Fig. 2

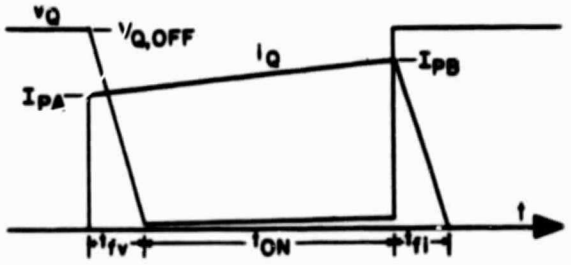


Fig. 3

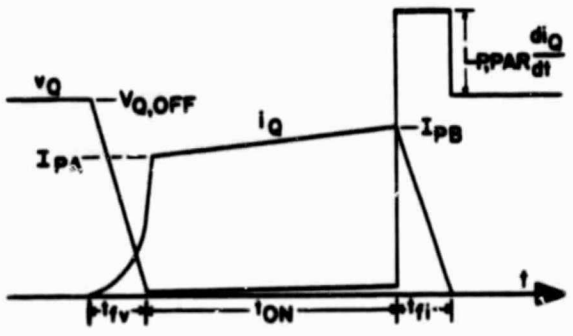


Fig. 4

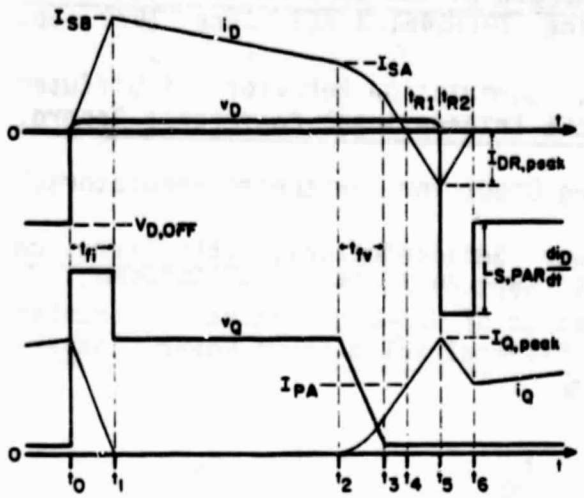


Fig. 5

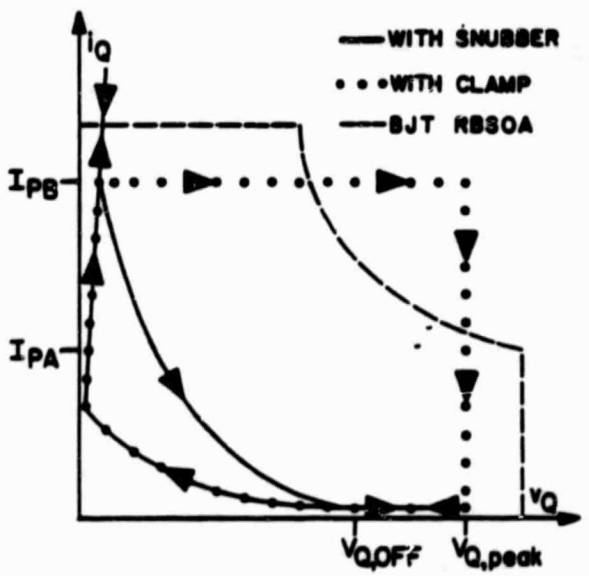
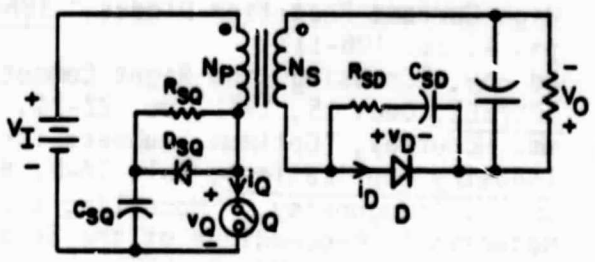
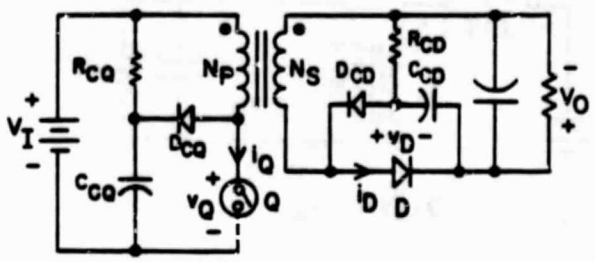


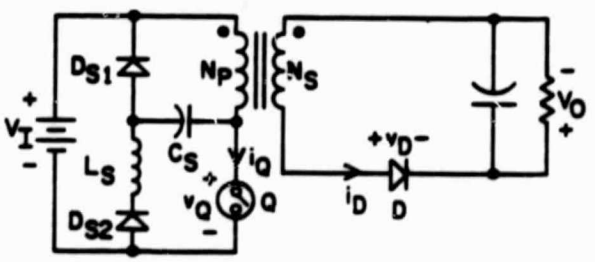
Fig. 7



(a)



(b)



(c)

Fig. 6